REMARKS/ARGUMENT

Support for the amendments made to the specification is located on page 7, lines 13-15 and Figure 2. No new matter has been introduced.

1) Claims 1, 2, 7 & 8 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Uesugi (6,295,445) in view of Nag et al (US 6,606,359). Applicant respectfully traverses this rejection, as set forth below.

In proceedings before the Patent and Trademark Office, "the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art". *In re Fritch*, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (citing *In re Piasecki*, 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). "The Examiner can satisfy this burden **only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references**", *In re Fritch*, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992)(citing *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988)(citing *In re Lalu*, 747 F.2d 703, 705, 223 USPQ 1257, 1258 (Fed. Cir. 1988)).

Similarly, "obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, **absent some teaching or suggestion supporting the combination. Under section 103, teachings of references can be combined ONLY if there is some suggestion or incentive to do so.**" *ACS Hosp. Systems, Inc. v. Montefiore Hosp.*, 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984).

Similarly, although couched in terms of combining teachings found in the prior art, the same inquiry must be carried out in the context of a purported obvious "modification" of

the prior art. **The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification.** *In re Gordon*, 733 F.2d at 902, 221 USPQ at 1127. Moreover, **it is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious.** *In re Gorman*, 933 F.2d 982, 987, 18 USPQ2d 1885, 1888 (Fed.Cir.1991). See also *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1138, 227 USPQ 543, 547 (Fed.Cir.1985).

Independent Claim 1, as amended, requires and positively recites, a receiver comprising: "analog-to-digital circuitry for generating a digital representation of a signal at an input", "adjustable gain control circuitry for receiving a radio signal and outputting an amplified analog signal using **a gain determined by a magnitude of the signal at an output** of the analog-to-digital circuitry" and "**digital channel filtering circuitry** for filtering said digital representation" and "digital processing circuitry for processing the output of said digital representation".

Independent Claim 7, as amended, requires and positively recites, a method of receiving a signal in a receiver, comprising the steps of: "generating a digital representation of a signal at an output of a analog-to-digital converter after applying a gain to the signal", "**adjusting the gain responsive to the magnitude of the digital representation of said output** of said analog-to-digital converter", "generating a **filtered digital representation** for a desired channel" and "processing the filtered digital representation".

In contrast, Uesugi discloses an automatic gain controlling apparatus and method designed to allow a received signal to be stable received level against the fluctuation of the

level of the received signal (see title & col. 1, lines 47-51). The Examiner readily admits that Uesugi fails to teach or suggest a digital channel filter (Office Action, page 3, lines 3-4). As such, Uesugi fails to teach or suggest, "**digital channel filtering circuitry** for filtering said digital representation", as required by Claim 1 AND "generating a **filtered digital representation** for a desired channel", as required by Claim 7.

Further, Uesugi's gain varying unit 3 does not adjust its gain in response to the magnitude of an output of A/D converting circuit 5b. Figure 2 discloses that an averaging process circuit 6 coupled the output of A/D converting circuit 5b to an input of fain varying unit 3. More specifically:

> The A/D converting unit 5 is connected to an **averaging process circuit** 6. The averaging process circuit 6 **averages the digital signal received from the A/D converting unit 5 in a predetermined time period T** and **controls the variable amount of the gain varying unit** 3 so that the digital signal converges at an N'bit digital value that represents a particular amplitude level (col. 4, lines 14-20).

Being that Uesugi uses an "average" of the digital signal received from the A/D converting unit in a predetermined time, it fails to teach or suggest, "adjustable gain control circuitry for receiving a radio signal and outputting an amplified analog signal using **a gain determined by a magnitude of the signal at an output** of the analog-to-digital circuitry", as required by Claim 1 AND "**adjusting the gain responsive to the magnitude of the digital representation of said output** of said analog-to-digital converter", as required by Claim 7. The Nag reference fails to provide any teaching that overcomes this deficiency of the Uesugi reference. For this reason alone, the 35 USC 103(a) rejection of Claims 1 and 7 is improper and should be withdrawn.

Even if, arguendo, Nag would have taught the above-identified deficiencies of the Uesugi reference, the additional fact that Nag discloses a digital channel filter 88 is not sufficient to make a determination that one having ordinary skill in the art at the time of the invention having Uesugi in front of him, would have next combined it with Nag to arrive at the invention of Applicant's Claims 1 and 7.

Applicant respectfully points out that the goal of the Nag reference was to provide a DC offset correction scheme. Figure 2 discloses that an output of A/D converter 66 if fed to Digital DC offset correction circuit 68, whose output is input to summing junction 60, which summed signal is fed back through to A/D converter 66. Circuit 68 calculates the average DC offset and corrects it, thereby generating the offset correction signal 76, which is an input to the summing junction 60 (col. 3, lines58-61). As such, the circuit is not concerned with compensating for variations in signal strength of a radio signal. Therefore, one having ordinary skill in the art would not have been motivated to combine this circuit with the teaching of Uesugi to arrive as the invention of Applicant's Claims 1 and 7. As such, the reasoning set forth by the Examiner is nothing more than improper hindsight reconstruction. Accordingly, the 35 U.S.C. 103(a) rejection of Claims 1 and 7 should be withdrawn.

Claims 2 and 8 stand allowable as depending from, respectively, allowable independent Claims 1 and 7 and by including further limitations not taught or suggested by the reference of record.

Claim 2 further defines the receiver of claim 1 wherein said analog-to-digital circuitry generates an output having a plurality of bit values and the gain applied by the adjustable gain control circuitry is determined responsive to one or more of the bit values. Claim 2 depends from Claim 1 and is therefore allowable for the same reasons set forth above for the allowance of Claim 1.

Claim 8 further defines the method of claim 7 and wherein said adjusting step comprises the step of adjusting the gain responsive to one or more bit values of said digital representation. Claim 8 depends from Claim 7 and is therefore allowable for the same reasons set forth above for the allowance of Claim 7.

2) Claims 3-5, 9 & 10 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Uesugi (6,295,445) in view of Nag et al (US 6,606,359) as applied to Claims 1 & 2 above, and further in view of Zamat (US 6,314,278). Applicant respectfully traverses this rejection, as set forth below.

In proceedings before the Patent and Trademark Office, "the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art". *In re Fritch*, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (citing *In re Piasecki*, 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). "The Examiner can satisfy this burden **only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references**", *In re Fritch*, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992)(citing *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988)(citing *In re Lalu*, 747 F.2d 703, 705, 223 USPQ 1257, 1258 (Fed. Cir. 1988)).

Similarly, "obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, **absent some teaching or suggestion supporting the combination. Under section 103, teachings of references can be combined ONLY if there is some suggestion or incentive to do so.**" *ACS Hosp. Systems, Inc. v. Montefiore Hosp.*, 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984).

Similarly, although couched in terms of combining teachings found in the prior art, the same inquiry must be carried out in the context of a purported obvious "modification" of the prior art. **The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification.** *In re Gordon*, 733 F.2d at 902, 221 USPQ at 1127. Moreover, **it is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious.** *In re Gorman*, 933 F.2d 982, 987, 18 USPQ2d 1885, 1888 (Fed.Cir.1991). See also *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1138, 227 USPQ 543, 547 (Fed.Cir.1985).

Claim 3 further defines the receiver of claim 2 wherein said gain is reduced by a first amount responsive to a most significant of said bit values indicating that the analog-to-digital converter has exceeded a first saturation threshold.

Claim 4 further defines the receiver of claim 3 wherein said automatic gain control circuit applies says first gain reduction independent of said digital processing circuitry.

Claim 5 further defines the receiver of claim 3 wherein said gain is reduced by a second amount responsive to a set of most significant bits of said bit values indicating that the analog-to-digital converter has exceeded a second saturation threshold.

Claim 9 further defines the method of claim 8 wherein said adjusting step includes the step of adjusting the gain by a first predetermined amount responsive to the value of a most significant bit of said bit values.

Claim 10 further defines the method of claim 9 wherein said adjusting step includes the step of adjusting the gain by a second predetermined amount responsive to a set of most significant bits of said bit values.

Claims 3-5 depend indirectly from Claim 1 and Claims 9 & 10 depend indirectly from Claim 7.

Independent Claim 1, as amended, requires and positively recites, a receiver comprising: "analog-to-digital circuitry for generating a digital representation of a signal at an input", "adjustable gain control circuitry for receiving a radio signal and outputting an amplified analog signal using **a gain determined by a magnitude of the signal at an output** of the analog-to-digital circuitry" and "**digital channel filtering circuitry** for filtering said digital representation" and "digital processing circuitry for processing the output of said digital representation".

Independent Claim 7, as amended, requires and positively recites, a method of receiving a signal in a receiver, comprising the steps of: "generating a digital representation of a signal at an output of a analog-to-digital converter after applying a gain to the signal", "**adjusting the gain responsive to the magnitude of the digital representation of said output** of said analog-to-digital converter", "generating a **filtered digital representation** for a desired channel" and "processing the filtered digital representation".

In contrast, Uesugi discloses an automatic gain controlling apparatus and method designed to allow a received signal to be stable received level against the fluctuation of the level of the received signal (see title & col. 1, lines 47-51). The Examiner readily admits that Uesugi fails to teach or suggest a digital channel filter (Office Action, page 3, lines 3-4). As such, Uesugi fails to teach or suggest, "**digital channel filtering circuitry** for filtering said digital representation", as required by Claim 1 AND "generating a **filtered digital representation** for a desired channel", as required by Claim 7.

Further, Uesugi's gain varying unit 3 does not adjust its gain in response to the magnitude of an output of A/D converting circuit 5b. Figure 2 discloses that an averaging process circuit 6 coupled the output of A/D converting circuit 5b to an input of fain varying unit 3. More specifically:

> The A/D converting unit 5 is connected to an **averaging process circuit** 6. The averaging process circuit 6 **averages the digital signal received from the A/D converting unit 5 in a predetermined time period T** and **controls the variable amount of the gain varying unit** 3 so that the digital signal converges at an N'bit digital value that represents a particular amplitude level (col. 4, lines 14-20).

Being that Uesugi uses an "average" of the digital signal received from the A/D converting unit in a predetermined time, it fails to teach or suggest, "adjustable gain control circuitry for receiving a radio signal and outputting an amplified analog signal using **a gain determined by a magnitude of the signal at an output** of the analog-to-digital circuitry", as required by Claim 1 AND "**adjusting the gain responsive to the magnitude of the digital representation of said output** of said analog-to-digital converter", as required by Claim 7. The Nag reference fails to provide any teaching that overcomes this deficiency of the Uesugi reference. For this reason alone, the 35 USC 103(a) rejection of Claims 1 and 7 is improper and should be withdrawn.

Even if, arguendo, Nag would have taught the above-identified deficiencies of the Uesugi reference, the additional fact that Nag discloses a digital channel filter 88 is not sufficient to make a determination that one having ordinary skill in the art at the time of the invention having Uesugi in front of him, would have next combined it with Nag to arrive at the invention of Applicant's Claims 1 and 7.

Applicant respectfully points out that the goal of the Nag reference was to provide a DC offset correction scheme. Figure 2 discloses that an output of A/D converter 66 if fed to Digital DC offset correction circuit 68, whose output is input to summing junction 60, which summed signal is fed back through to A/D converter 66. Circuit 68 calculates the average DC offset and corrects it, thereby generating the offset correction signal 76, which is an input to the summing junction 60 (col. 3, lines58-61). As such, the circuit is not concerned with compensating for variations in signal strength of a radio signal. Therefore, one having ordinary skill in the art would not have been motivated to combine this circuit with the teaching of Uesugi to arrive as the invention of Applicant's Claims 1 and 7.

Similarly, even if, arguendo, the Zamat reference teaches that gain is reduced by a first amount responsive to a most significant of said bit values indicating that the analog to digital converter has exceeded a first saturation threshold (as suggested by the Examiner at page 3, line 22 – page 4, line 3), Zamat fails to teach the above-identified deficiencies of the combination of the Uesugi and Nag references. Further, even if Zamat would have supplied such deficiencies in Uesugi and Nag, the Examiner has presented no evidence from the prior art that one having ordinary skill in the art would have been motivated to combine Uesugi, Nag with Zamat "in order to make the system more efficient". Such determination seems to be using Applicant's disclosure as a template to piece together the prior art in order to obviate the claims, which is not permitted by law. Accordingly, the 35 USC 103(a) rejection of Claims 3-5, 9 and 10 is improper and should be withdrawn.

3) Claim 6 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Uesugi (6,295,445) in view of Nag et al (US 6,606,359) as applied to Claims 1 & 2 above, and further in view of Sasaki (US 6,314,278). Applicant respectfully traverses this rejection, as set forth below.

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Claim 6 further defines the receiver of claim 2 wherein said gain is increased responsive to a set of most significant bits of said bit values indicating that the analog-to-digital converter is below a threshold.

Claim 6 depend indirectly from Claim 1.

Independent Claim 1, as amended, requires and positively recites, a receiver comprising: "analog-to-digital circuitry for generating a digital representation of a signal at an input", "adjustable gain control circuitry for receiving a radio signal and outputting an amplified analog signal using **a gain determined by a magnitude of the signal at an output** of the analog-to-digital circuitry" and "**digital channel filtering circuitry** for filtering said digital representation" and "digital processing circuitry for processing the output of said digital representation".

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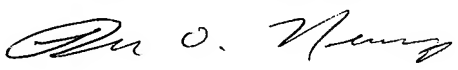
Even if, arguendo, Nag would have taught the above-identified deficiencies of the Uesugi reference, the additional fact that Nag discloses a digital channel filter 88 is not sufficient to make a determination that one having ordinary skill in the art at the time of the invention having Uesugi in front of him, would have next combined it with Nag to arrive at the invention of Applicant's Claims 1.

Applicant respectfully points out that the goal of the Nag reference was to provide a DC offset correction scheme. Figure 2 discloses that an output of A/D converter 66 if fed to Digital DC offset correction circuit 68, whose output is input to summing junction 60, which summed signal is fed back through to A/D converter 66. Circuit 68 calculates the average DC offset and corrects it, thereby generating the offset correction signal 76, which is an input to the summing junction 60 (col. 3, lines58-61). As such, the circuit is not concerned with compensating for variations in signal strength of a radio signal. Therefore, one having ordinary skill in the art would not have been motivated to combine this circuit with the teaching of Uesugi to arrive as the invention of Applicant's Claim 1.

Similarly, even if, arguendo, the Sasaki reference were to teach that gain is increased responsive to a set of most significant bits of said bit values indicating that the analog to digital converter is below a threshold (as suggested by the Examiner at page 4, line 22 – page 5, line 2), Sasaki fails to teach the above-identified deficiencies of the combination of the Uesugi and Nag references. Further, even if Sasaki would have supplied such deficiencies in Uesugi and Nag, the Examiner has presented no evidence from the prior art that one having ordinary skill in the art would have been motivated to combine Uesugi, Nag with Sasaki "to include an increased gain correlated to a threshold value, such as that taught by Sasaki, in order to maintain a more steady signal output". Such determination seems to be using Applicant's disclosure as a template to piece together the prior art in order to obviate the claims, which is not permitted by law. Accordingly, the 35 USC 103(a) rejection of Claim 6 is improper and should be withdrawn.

Claims 1-10 stand allowable. New Claims 11-21 are similarly allowable. Applicants respectfully request withdrawal of the rejections and allowance of the application at the earliest possible date.

Respectfully submitted,



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